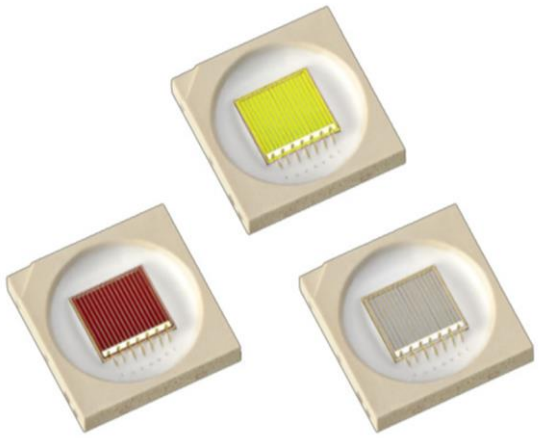
Design Guidelines for SFT Chipsets Assembly

SFT-10
SFT-16
SFT-20



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Introduction

The high performance Luminus SFT window-less LED chipsets enable cost effective solutions for coloring or white lighting, including Pico projection, automotive, entertainment, fiber illumination, emergency lighting, and beacons.

For high current density operation of SFT chipsets, thermal management is critical in application design. This application note will describe the basic design guidelines, provide available reference designs and comparison among several configurations about SFT chipsets application.

Scope

The design guidelines in this application note apply to all the SFT chipsets with part number SFT-xx-y where:

xx- for emitter size 10 – 1.0 mm^2, 16 – 1.6 mm^2, and 20 – 2.0 mm^2;

y – for product color RA – red amber; CG – converted green, G – Green, B – Blue, and W – White.

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1. Design Guidelines

1.1 Electrical Insulation

The SFT chipsets are ultra-compact, surface mount, high-power LEDs. Each SFT chipset consists of a high brightness LED chip on a EMC frame. The EMC frame provides mechanical support and a thermal path from the LED chip to the bottom of chipset. There are 2 electrical pads on the bottom of the EMC frame with a spacing of 0.43 mm between them. The larger pad serves as both cathode and thermal pad. The smaller pad is anode pad only providing electrical connection to LED chip.

In order to avoid any electrical shock and/or damage to the SFT chipsets, each design needs to comply with the appropriate standards of safety and insulation distances. A recommended solder pad layout could be found in both the product datasheet and mechanical drawing.

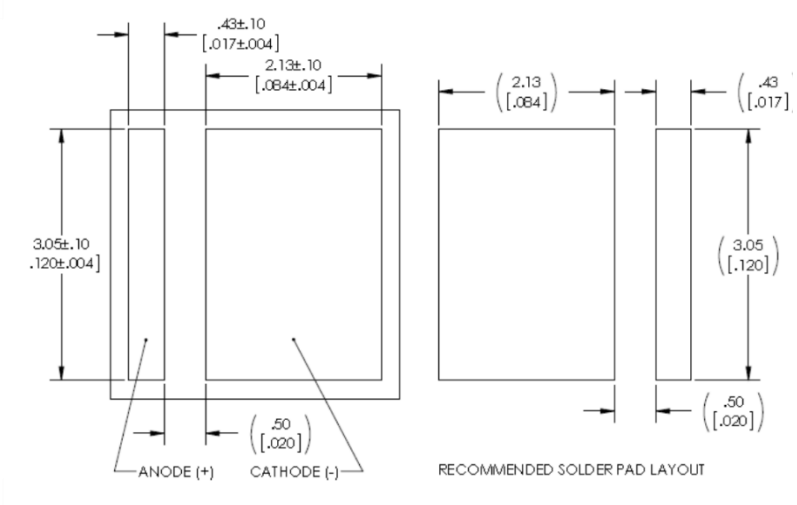

Fig.1 Electrical pinout and recommended solder pad layout

Since the thermal pad is electrically active, electrical insulation for SFT chipsets will be required in customer application. The electrical insulation could be achieved with four configurations. These configurations are listed in order of best performance:

Configuration 1.A No insulation, as shown in Fig. 2(a). If customer has a LED driver which can handle common cathode design, it is not necessary to have LEDs insulated from the system. However, this configuration requires pedestal design on PCB. With a pedestal PCB, LED cathode will be connected with PCB and heatsink directly without a dielectric layer in between. Customer can simply keep the heatsink grounded with LED driver circuit.

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Configuration 1.B system level insulation, as shown in Fig. 2(b). When pedestal PCB is used for SFT chipsets assembly, customer might not be able to drive SFT chipsets with a common cathode LED driver. In that case, insulation could be archived by electrically isolating heatsink from the rest of the system.

Configuration 2 PCB level insulation, as shown in Fig. 2 (c). With a pedestal PCB, the back side and sidewall of PCB are electrically active. A layer of electrically insulating thermal interface material (TIM) will be helpful to keep SFT chipsets insulated at PCB level;

Configuration 3 packaging level insulation, as shown in Fig. 2(d). Electrical insulation can also be achieved by using a global dielectric layer on PCB. This configuration is NOT recommended for any high current density (A/mm^2) application of SFT chipsets due to reduced thermal performance. However, we will still describe the details about this configuration the section of "Available Reference Designs for Thermal Management Configurations", for those customers whose system does not allow all the 3 configurations (1A, 1B and 2) described above.

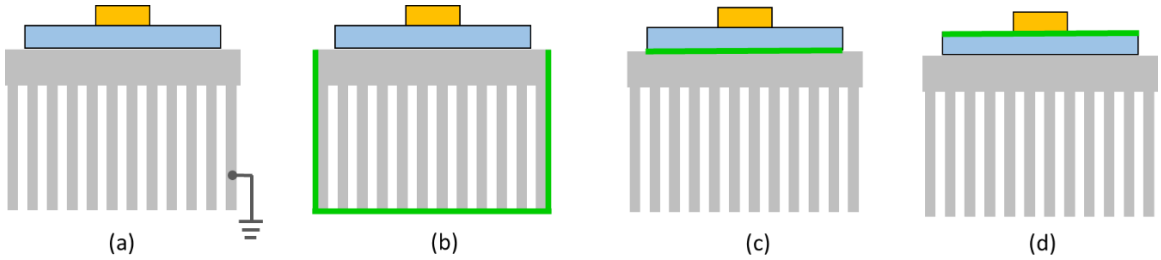

Fig. 2 Electrical insulation options for SFT chipsets. Green line/frame indicate electrical insulation material in the system. (a) Config.1A No insulation/common cathode; (b) Config. 1B system level insulation; (c) Config. 2 PCB level insulation; (d) Config. 3 Packaging level insulation.

Based on the assumption that heatsink periphery will cool down to ambient temperature, in thermal management prospective the configuration of no insulation (Config. 1A) and system level insulation (Config. 1B) are thermally equivalent. We will group them together as Config.1 during the rest of discussion about thermal management.

1.2 Thermal Management

Given that SFT chipsets will need some level of insulation, and LED performance highly depends on operating temperature, a good thermal management is critical for SFT chipsets to get satisfying performance.

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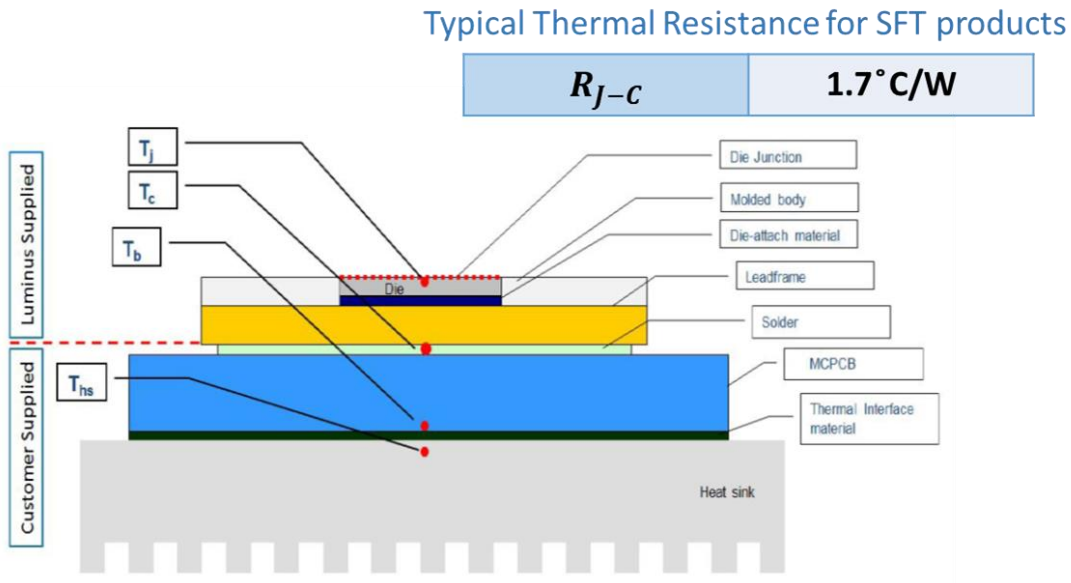

Fig. 3 Thermal resistance for SFT-20 chipsets

We have a detailed description about thermal analysis method in the application note of "Thermal Management Application Note". You can also find that part in Appendix A- thermal analysis basics at the end of this application note.

Here let us start the discussion about SFT chipsets with system thermal resistance for each thermal management configuration. For the 3 configurations of SFT assembly design, the system thermal resistance would be:

Config. 1: No insulation or system level insulation

$$R_{\theta j-amb} = R_{J-C} + R_{Solder} + R_{PCB} + R_{thermal\ grease} + R_{heatsink}$$

Config. 2: PCB level insulation

$$R_{\theta j-amb} = R_{J-C} + R_{Solder} + R_{PCB} + R_{insulating\ TIM} + R_{heatsink}$$

Config. 3: Packaging level insulation

$$R_{\theta j-amb} = R_{J-C} + R_{Solder} + R_{copper\ trace} + R_{dielectric\ layer} + R_{PCB} + R_{thermal\ grease} + R_{heatsink}$$

Table. 1 provided simulation results for different thermal management configurations, assuming the same SFT-20-RA, operating at the same maximum condition (I = 8 A, V_f= 3.5 V, Duty cycle 25%) at a same ambient temperature of 40℃. It is clear that Config. 1 gives the lowest value of thermal resistance and junction temperature, which indicates that Config.1 is the most favorable option in term of thermal management. Three reference designs will be described in next section with further detail.

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Table 1. System thermal resistance for different thermal management configurations

Config.	Description	R_{j-c} [℃/W]	R_{j-h} [℃/W]	LED Power [W]	T_j [℃]
1	No insulation or system level insulation	1.7	2.4	7.0	56.6
2	PCB level insulation	1.7	4.5	7.0	71.7
3	Package level insulation	1.7	5.5	7.0	78.6

2. Available Reference Designs for Thermal Management Configurations

2.1 Config. 1: No insulation or system level insulation

In this configuration, the heatsink is well thermally-connected with SFT chipsets and provides optimized heat conduction. SFT chipsets operating in this configuration, compared with SFT chipsets operating in other configurations, will have the best performance, reliability and lifetime. We strongly encourage customer to design their system with this configuration.
A key design detail for this configuration is the pedestal design of PCB.

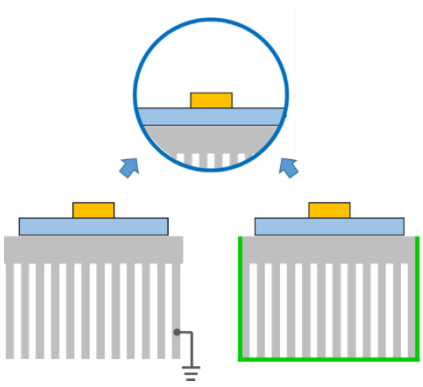

Fig. 4 No insulation or system level insulation

Pedestal design of PCB: As shown in Fig. 5, there are 3 small areas standing higher than the rest part of the PCB base. And, the dielectric layer is patterned as well, leaving the pedestal area exposed for electrical connection. In this way, the cathode solder pad on a SFT chipset is connected to the pedestal copper directly and serves as a thermal pad, transferring heat into the body of PCB efficiently and without any heat transfer congestion.
Another benefit of SFT chipset assembly on pedestal PCB is, by raising the PCB base at the location of common cathode/thermal pad, the thermal pad on SFT chipset can sit on a thinner solder layer which lead to better heat conduction through solder layer. Fig. 6 shows the comparison between SFT chipset assembly on pedestal PCB and a similar LED chipset without using pedestal PCB.

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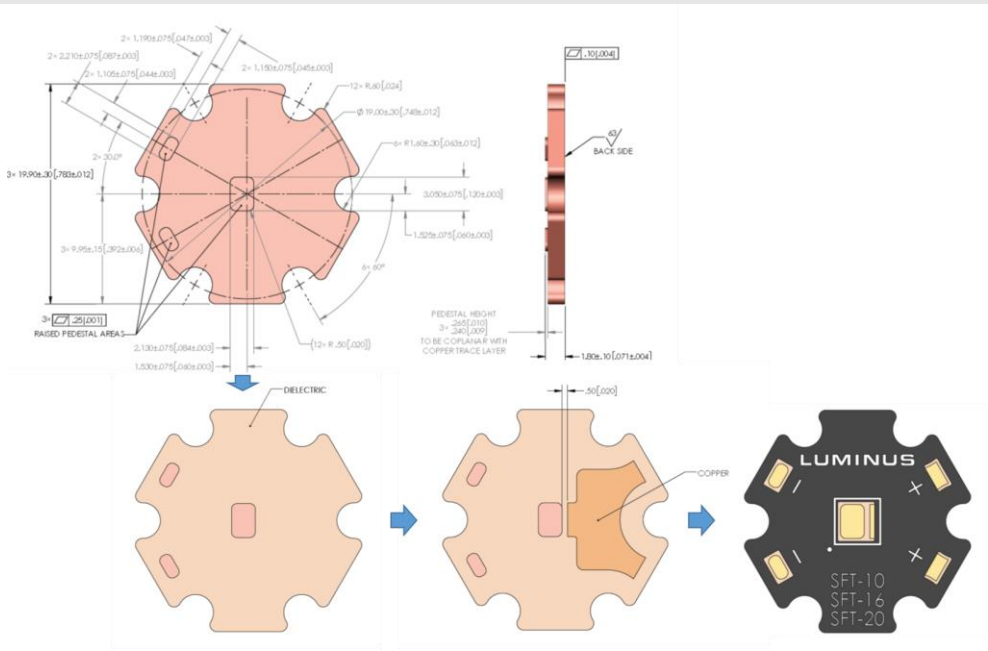

Fig. 5 Reference pedestal PCB design (please refer to DWG-400845 for further detail)

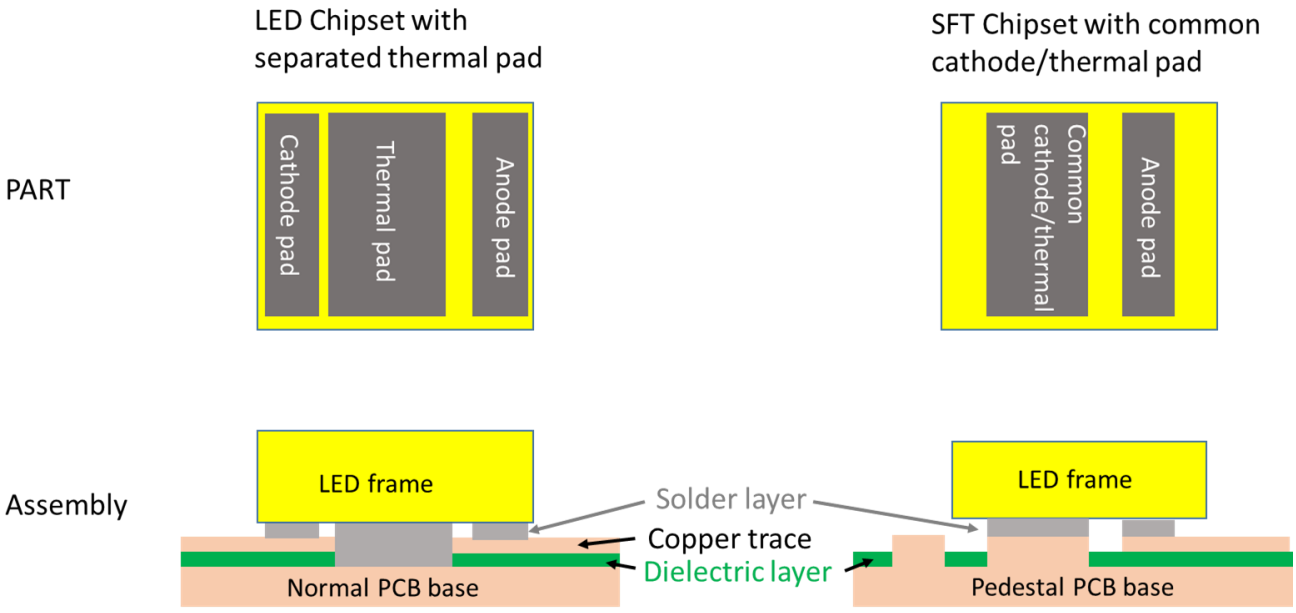

Fig. 6 LED chipset assembly on PCB

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The star board shown in Fig. 5 could be found with our distributor with the part number of "Starboard SFT-10/16/20-RGBW pedestal". Rayben, as our PCB partner, will be able to provide support for customized pedestal PCB design and manufacture.

2.2 Config. 2: PCB level insulation

When pedestal PCB is used, but customer has difficulty to use either common cathode LED driver or system level insulation, electrically-insulating TIM will be another option we would suggest. Among all TIMs, electrically-insulating TIMs usually do not have the best thermal performance. This is the reason why Config.2 will not as optimized as Config. 1. However, benefited by pedestal PCB, the entire metal body of PCB can still help SFT chipsets to maintain a reasonable operating junction temperature T_j and lumen output.

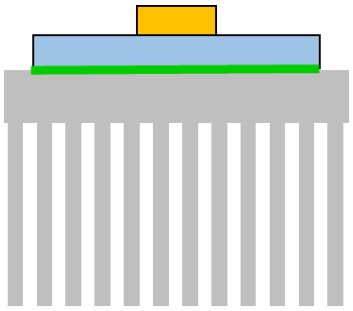

Fig. 2 (c) PCB level insulation

Electrically-Insulating TIM: With pedestal PCB the back side of PCB is electrically active. To achieve electrical insulation right underneath PCB, we recommend insulating TIM such as 3M Pad 5590PI which has a thermal conductivity of 3.0 W/m-K, and a thickness of 200 μm (https://media.digikey.com/pdf/Data%20Sheets/3M%20PDFs/5590PI.pdf). Any other electrically-insulating TIM with a thermal conductivity HIGHER than 3.0 W/m-K or a thickness LESS than 200 μm would be considered suitable for SFT chipsets.

Assembly accessory: For the design of PCB level insulation, not only the back side, but the sidewall of PCB is also electrically active. We recommend plastic washer and sleeve for PCB installation on heatsink. This will ensure that electrical shock won't occur between sidewall of PCB and heatsink.

2.3 Config. 3: Package level insulation

When electrical insulation has to be achieved at package level, a global dielectric layer on top of the metal PCB will be needed. In this configuration, the cathode solder pad will be sitting on top of a solder material layer, a copper trace layer and a dielectric layer, before heat could be conducted to PCB. This thermal path will NOT be efficient enough for a SFT package, especially for high current density application. We do NOT recommend this configuration. However, we will still describe the design details for this configuration, for those customers who have difficulty to implement all other configurations.

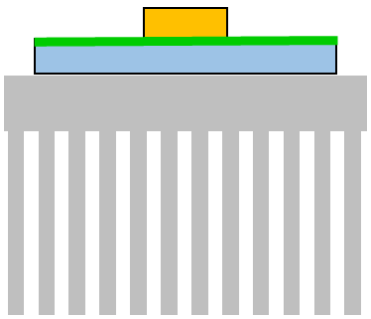

Fig. 2 (d) Packaging level insulation

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Due to the challenge of thermal management, the parameters of dielectric layer and circuit layer copper trace are both critical.

Dielectric layer: Most default dielectric material provided by PCB suppliers is not efficient enough for SFT chipset's thermal management. The dielectric layer should be thin enough and have a thermal conductivity high enough to allow heat conduction. We recommend Bergquist HLP material (http://www.bergquistcompany.com/thermal_substrates/LEDs/hpl.html) , with a thermal conductivity of 3.0 W/m-K, and a thickness of 38 μm. A dielectric layer has a thermal conductivity HIGHER than 3.0 W/m-K or a thickness LOWER than 38 μm would be suitable for SFT chipset application.

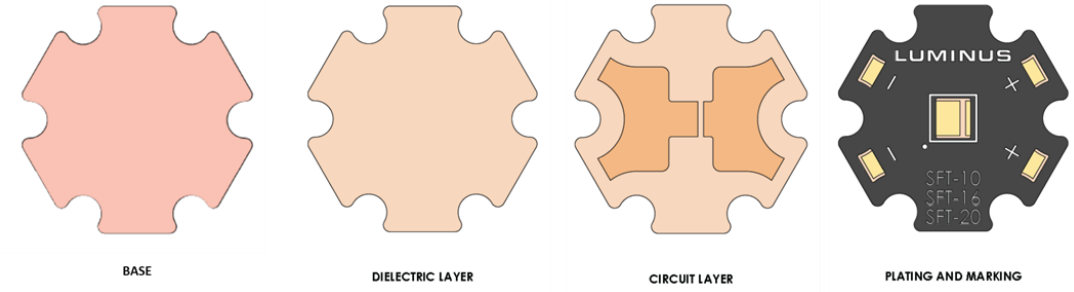

Fig. 6 Reference PCB design (please refer to DWG-400832 for further detail)

Copper trace: for this configuration, a suitable dielectric layer can only conduct part of the heat generated by a SFT chipset. A large portion of heat needs to be conducted through the copper trace on top of dielectric layer. We have tested different variations of thickness of copper traces on top of a global Bergquist HLP layer. Our study shows, the minimum requirement of copper trace could be 2 oz (75 μm in thickness). The cathode trace areas showed in the reference design is the minimum requirement. A larger trace area for cathode would be preferred.

The star board shown in Fig. 6 could be found with our distributor with the part number of "Starboard SFT-10/16/20-RGBW".

2.4 Comparison of thermal management configurations

According to Tab.1, different configurations perform differently in term of thermal management. Our testing results show, that SFT chipsets performance is significantly affected by its thermal operation condition. In Tab. 2, the performance drop in different configurations are used for SFT-20 RGB chipsets operating at maximum power. Since Config.1 is the most optimized operation condition, the lumen loss of other configurations is compared with Config.1.

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Table 2 Comparison between reference designs

SFT-20-RA @ 8A/3.5V/25% DC/ $T_{heatsink}$ 40 ▫C					
Config.	**Description[2]**	**System thermal resistance[3] R_{j-h} [℃/W]**	**P_{LED} [W]**	**T_j [℃]**	**Lumen output loss[1]**
1	No insulation or system level insulation	2.38	7	56.7	0.00%
2	PCB level insulation	4.53	7	71.7	13.9%
3	Package level insulation	5.51	7	78.6	20.2%
SFT-20-CG @ 8A/3.7V/50% DC/ $T_{heatsink}$ 40 ℃					
Config.	**Description[2]**	**System thermal resistance[3] R_{j-h} [℃/W]**	**P_{LED} [W]**	**T_j [℃]**	**Lumen output loss [1]**
1	No insulation or system level insulation	2.38	14.8	75.2	0.00%
2	PCB level insulation	4.53	14.8	107.0	6.4%
3	Package level insulation	5.51	14.8	121.6	9.3%
SFT-20-B@ 8A/3.7V/25% DC/ $T_{heatsink}$ 40 ▫C					
Config.	**Description[2]**	**System thermal resistance[3] R_{j-h} [℃/W]**	**P_{LED} [W]**	**T_j [℃]**	**Lumen output loss[1]**
1	No insulation or system level insulation	2.38	7.4	57.612	0.0%
2	PCB level insulation	4.53	7.4	73.522	3.2%
3	Package level insulation	5.51	7.4	80.774	4.6%
SFT-20-W @ 4A/3.7V/CW 100% DC/ $T_{heatsink}$ 40 ℃					
Config.	**Description[2]**	**System thermal resistance[3] R_{j-h} [℃/W]**	**P_{LED} [W]**	**Tj [℃]**	**Lumen output loss[1]**
1	No insulation or system level insulation	2.38	14.8	75.2	0.0%
2	PCB level insulation	4.53	14.8	107.0	6.4%
3	Package level insulation	5.51	14.8	121.6	9.3%

Note:

1. LED cold-hot factor: RA 0.92 %/ ℃; Blue, CG and White 0.20 %/ ℃, CG and white have the same cold – hot factor because they are both built on blue LED chip;
2. System detail of each configuration includes:
   Config. 1: Pedestal 1.8mm copper PCB
   Config. 2: Pedestal 1.8mm copper PCB, Electrically Insulating TIM (3M)
   Config. 3: 2oz Cu trace, Dielectric 38um (3.0W/m-k), Cu base 1.8mm
3. In this simulation a constant Rj-h =1.7 ℃/ W for is used different color (R, CG, B and W), which is the worst case in thermal analysis. Our internal testing on prototype SFT-20 shows CG, B and W might have a smaller thermal resistance.

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3. System Level Performance Simulation

We also simulated the system performance based on Config.1. With the most optimized thermal management configuration, we can get around 265 lm @ 18W with ~30% light engine efficiency. If light engine efficiency can reach 32.5% and have capability to dissipate ~20W, then we can get over 300lm at light engine level. Detailed results are listed in Tab. 3.

Tab. 3 Projector performance simulation with SFT-20 chipsets

Parameters	0.3'' 720P TRP Projector Q4/16					
DMD Panel	0.3" 720P/F#1.7			0.3" 720P/F#1.7		
LED Light Engine	SFT20/30% Light Engine @18W			SFT20/32.5% Light Engine @ 20W		
RGB Colors	Red	PC-Green	Blue	Red	PC-Green	Blue
LED Output Bin @1.4A/mm2 [lm]	1C	2C	4C	1C	2C	4C
System driving current [A]	4.0	5.90	5.90	5.0	6.3	6.0
LED Output @ system current [lm]	539	1282	233	565	1380	240
Voltage [V]	3.17	3.35	3.47	3.20	3.40	3.48
Duty Cycle w/o overlap	28.0%	56.0%	16.0%	28.0%	56%	16.0%
RGB LED Lumens	151	718	37	158	773	38
Thermal de-rating & blue absorption	90%	98%	86%	90%	98%	86%
Dominant Wavelength [nm]	613	525	460	613	525	460
RGB Power Consumption [W]	3.550	11.068	3.276	4.480	11.995	3.341
Total LED Power [W]	17.9			19.8		
Total Source White Lumens [lm]	871			933		
Light Engine Efficiency	30.4%			32.5%		

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RGB Output Lumens [lm] on Screen	41.25	213.62	9.72	46.25	246.07	10.73
Light Engine Output w/o overlap Typ [lm]	264.6			303		
Light Engine Overall Efficacy [lm/W]	14.79			15.29		

4. Temperature Monitoring

In order to ensure SFT chipsets are operating under a preferred condition, we recommend customer to test SFT chipsets in prototype system. For temperature monitoring, we suggest customer to measure the LED solder joint temperature using a thermal couple attached to PCB close to the solder point. An accurate solder joint temperature T_s could be acquired with this setup. T could be easily calculated with the equation of

$$T_j = R_{j-c} \times P_{LED} + T_s$$

When operating wavelength and lumen output are different than expectation, please check thermal condition of SFT chipsets.

5. Recommended Testing Approach

A lot times, customer would like to test and approve product performance with their in-house testing system. The data in table 2 could explain that when testing condition is not carefully set, SFT chipsets performance would be very different from the parameters provided by product datasheet.

The datasheet of SFT chipsets are tested at $T_j = 40\ ℃$. The right way to duplicate the testing result is to:

1. Install LED onto a temperature-controlled stage at $40\ ℃$ for optical measurement;
2. Light up the LED with a short pulse and get a correct reading of the pulse.

Due to the capability of high current density operation, SFT chipsets could be damaged within a few second if lacking of required thermal management.

For any questions about data and material described in this application note, or further possible SFT chipsets thermal management, please contact techsupport@luminus.com. Thank you for choosing Luminus Devices.

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6. Appendix A

6.1 Thermal Analysis Basics

When designing thermal management for SFT LEDs, the primary objective is to determine the junction temperature of the LED at operation condition. The simplest method to determine the temperature is to use thermal resistances.

A thermal management system can be thought of as a series system thermal resistors extending from the LED p-n junction to the ambient, as shown in Fig 3. Each material or interface has some resistivity to thermal transfer and contributes to the total thermal resistance of the system. Since the primary goal of the thermal management system is to minimize the LED junction temperature, the lowest possible system thermal resistance value is desired.

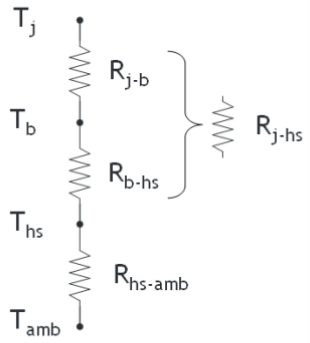

Fig. 3 Series thermal resistance

The thermal resistance between any two points is defined as the ratio of the difference in temperature between the two points and the power dissipated. Thus, for the thermal resistance between LED junction and the ambient environment, this relationship is given by:

$$R_{\theta j-amb} = \Delta T_{j-amb}/P_{Diss}$$

Where:

$R_{\theta j-amb}$: Thermal resistance from LED junction to ambient

ΔT_{j-amb}: Temperature difference between LED junction and ambient

P_{Diss}: Dissipated Power: Drive current × Forward voltage (× Duty Cycle)

Note: The amount of power dissipated optically is neglected in this calculation.

In many cases, the thermal resistance of parts of the system are already known. Therefore, it is useful to rearrange the thermal resistance equation to solve for junction temperature:

$$T_j = R_{\theta j-amb} \times P_{Diss} + T_{amb}$$

From this equation, we see that the necessary values to calculate junction temperature are:

1. Thermal resistance from junction to ambient
2. Power dissipated from the LED
3. Ambient temperature of the surrounding environment

Given information about the system and the LED drive condition, this basic equation allows the designer to determine the operation LED junction temperature.

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